

521,397
Rec'd PCT/PTO 14 JAN 2005

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property
Organization
International Bureau



10/521397



(43) International Publication Date
29 January 2004 (29.01.2004)

PCT

(10) International Publication Number
WO 2004/010212 A1

(51) International Patent Classification⁷: G02F 1/1337

(21) International Application Number:
PCT/KR2002/001782

(22) International Filing Date:
19 September 2002 (19.09.2002)

(25) Filing Language: Korean

(26) Publication Language: English

(30) Priority Data:
2002/42658 19 July 2002 (19.07.2002) KR

(71) Applicant (for all designated States except US): SAMSUNG ELECTRONICS CO., LTD. [KR/KR]; 416, Maetan-dong, Paldal-ku, 442-370 Suwon-city, Kyungki-do (KR).

(72) Inventors; and

(75) Inventors/Applicants (for US only): CHOI, Young-Min

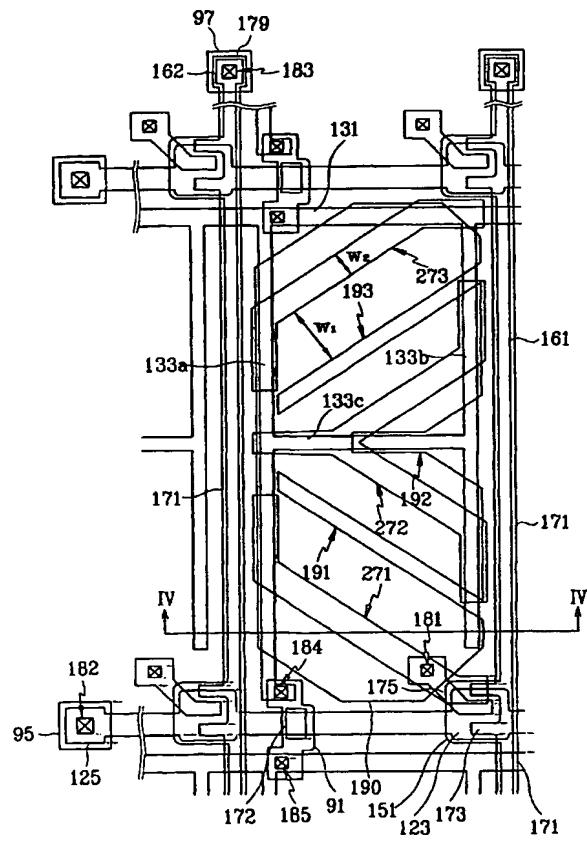
[KR/KR]; Seoju Building 403, 1357-21, Seocho 2-dong, Seocho-ku, 137-072 Seoul (KR). SONG, Jang-Kun [KR/KR]; Samik Apt. 5-201, Seocho 4-dong, Seocho-ku, 137-778 Seoul (KR). KIM, Jin-Yun [KR/KR]; Shinjeong Maeul Jookong 1-danji Apt. 109-504, 1065, Pondon-dukcheon-ri, Suji-eup, 449-846 Yongin-city, Kyungki-do (KR).

(74) Agent: YOU ME PATENT & LAW FIRM; Teheran Bldg., 825-33, Yoksam-dong, Kangnam-ku, 135-080 Seoul (KR).

(81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

[Continued on next page]

(54) Title: VERTICALLY ALIGNED MODE LIQUID CRYSTAL DISPLAY



(57) Abstract: A liquid crystal display is provided, which includes: a first insulating substrate; a gate line formed on the first insulating substrate; a gate insulating layer formed on the gate line; a data line formed on the gate insulating layer; a passivation layer formed on the data line; a pixel electrode formed on the passivation layer and a first cutout pattern; a second insulating substrate facing the first insulating substrate; and a common electrode formed on the second insulating substrate and having a second cutout pattern, wherein width of the domains is equal to or less than 30 microns.

WO 2004/010212 A1